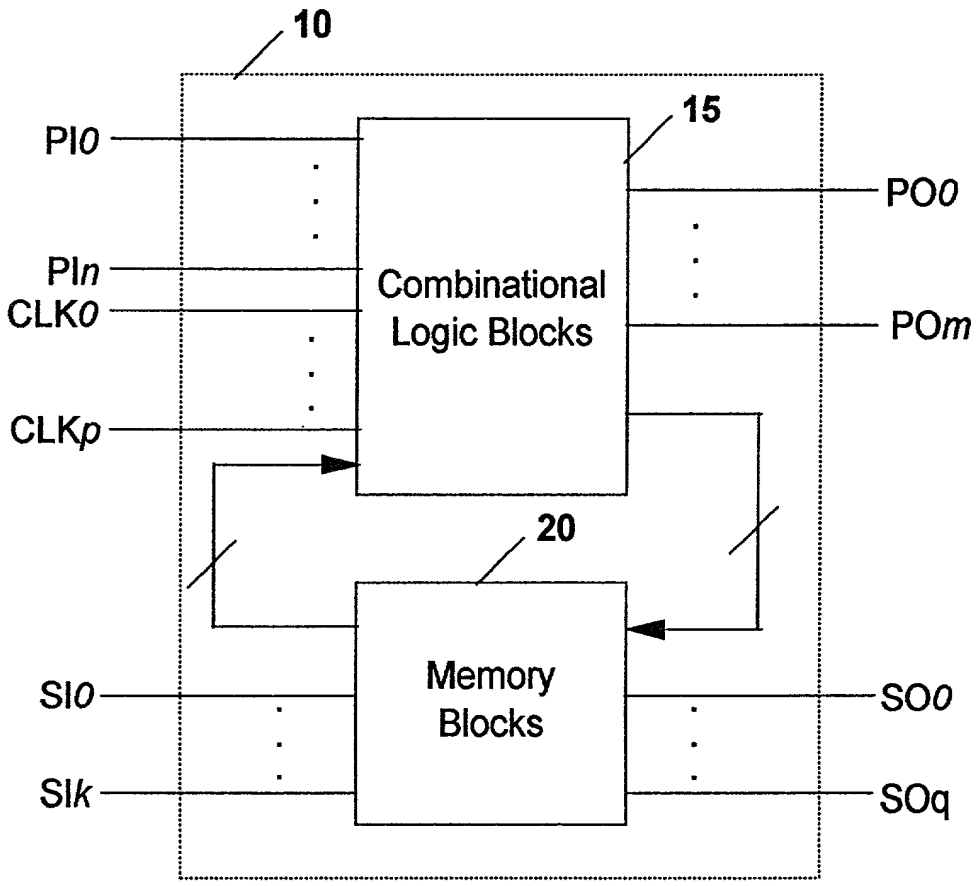

10
15
PI0
PIn
CLK0
CLKp
Combinational
Logic Blocks
PO0
POm
20
Memory
Blocks
SI0
SIk
SO0
SOq

Figure 1.

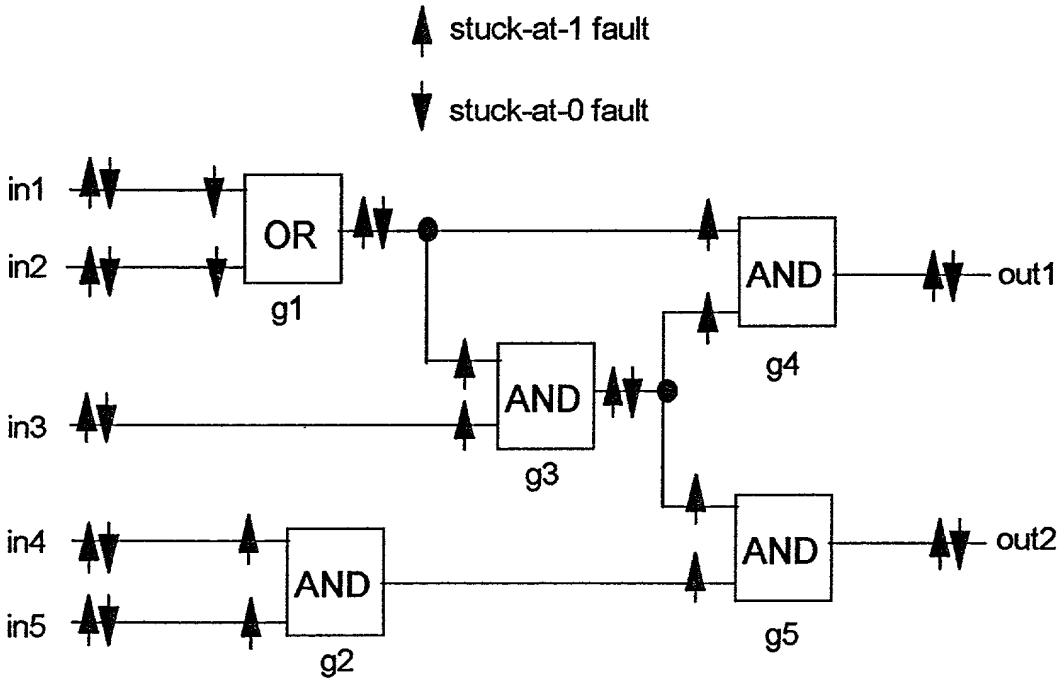

stuck-at-1 fault
stuck-at-0 fault
in1
in2
in3
in4
in5
OR
g1
AND
g2
AND
g3
AND
g4
AND
g5
out1
out2

Figure 2.

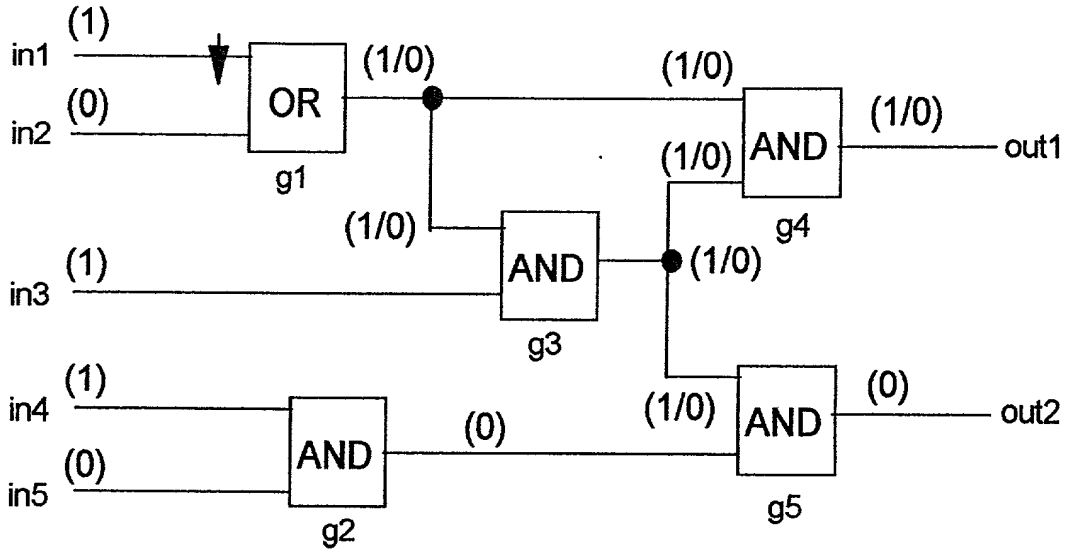


Figure 3.

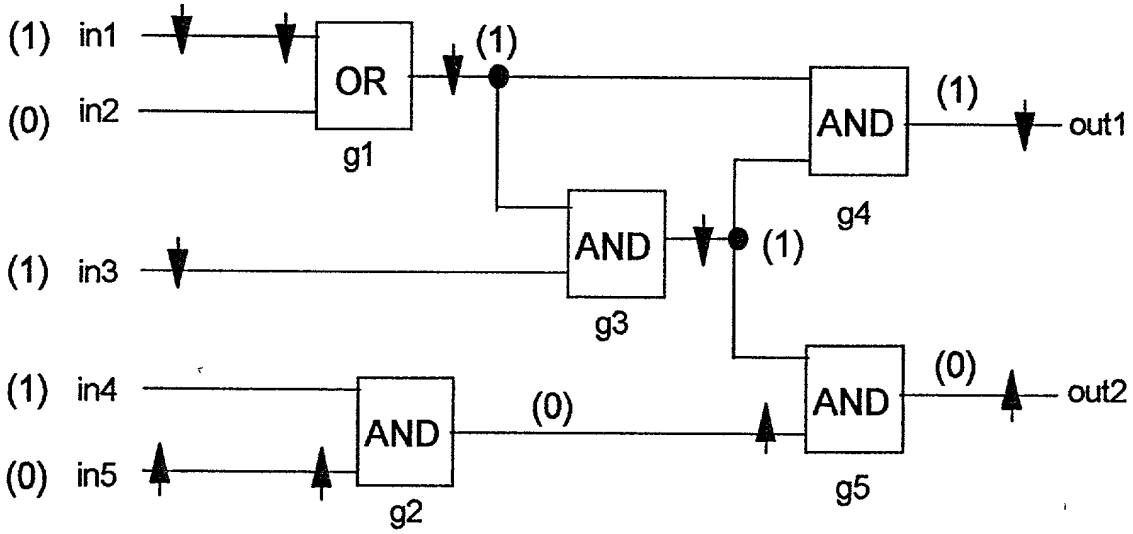


Figure 4.

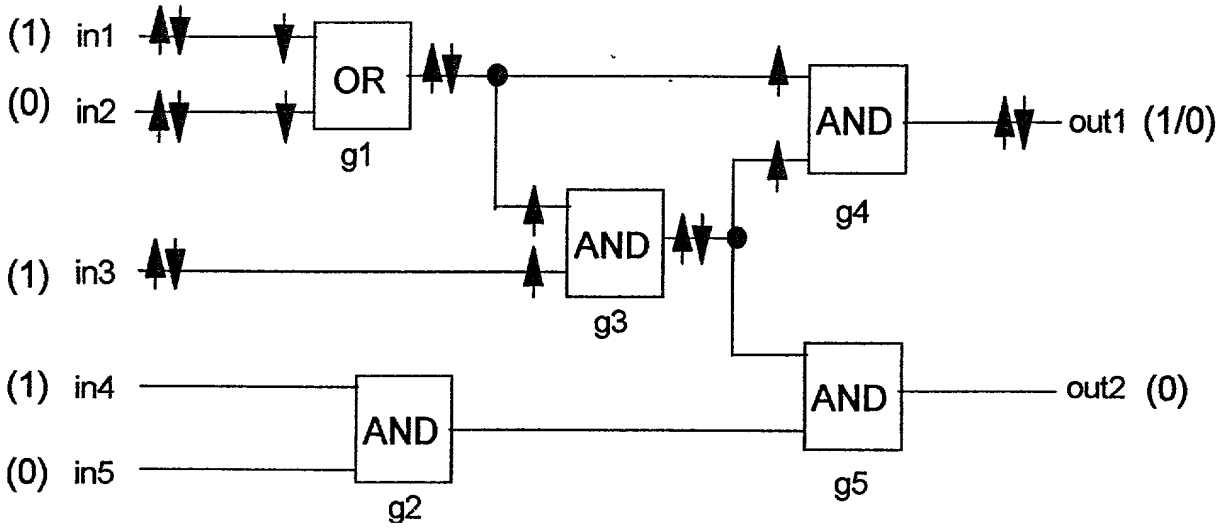


Figure 5

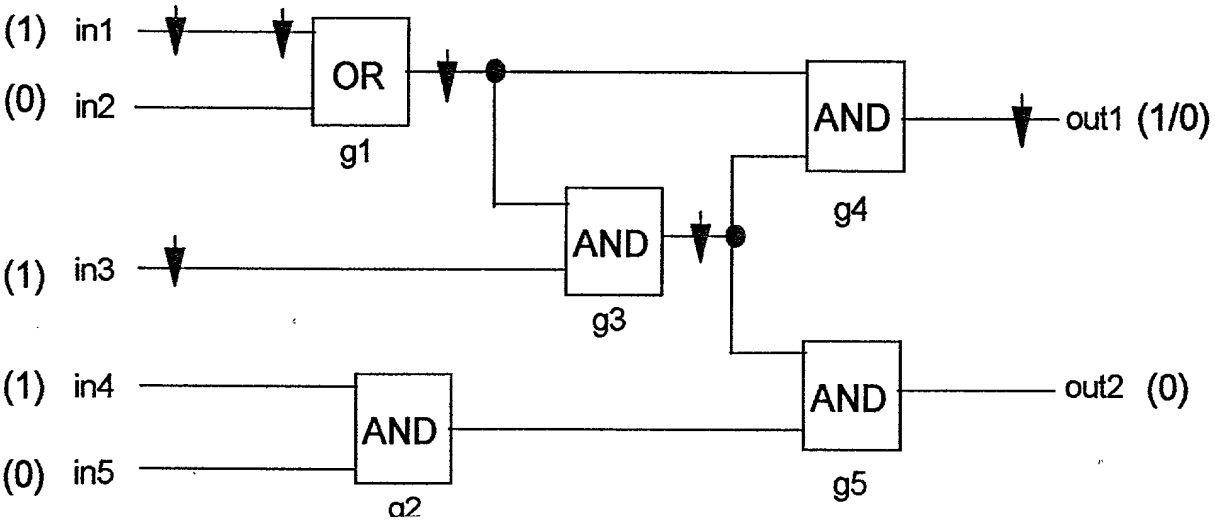


Figure 6.

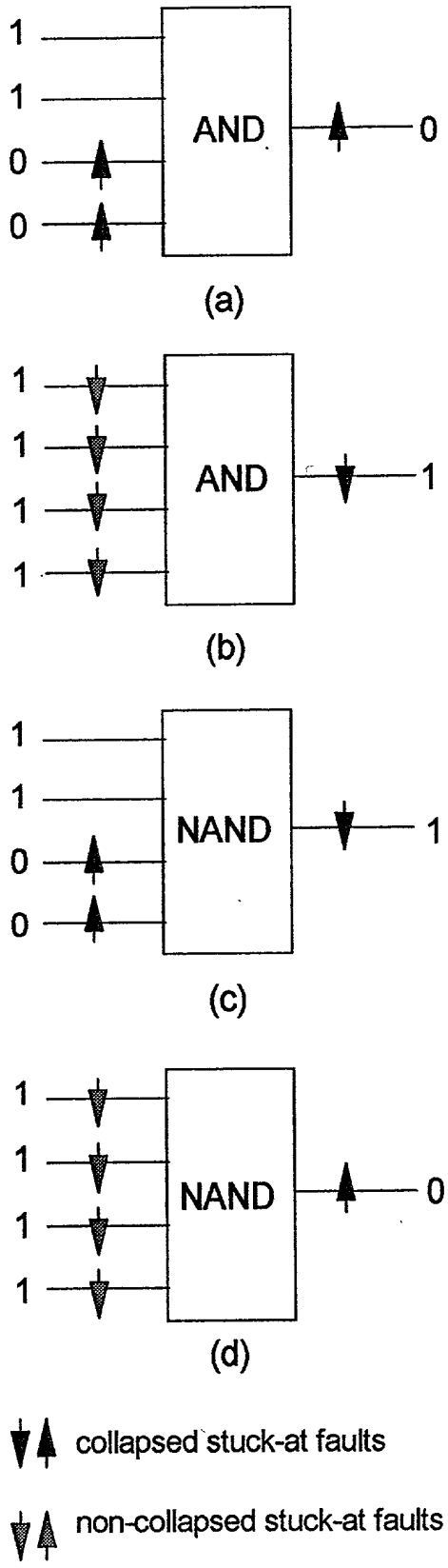

1
1
0
0
AND
0
(a)
1
1
1
1
AND
1
(b)
1
1
0
0
NAND
1
(c)
1
1
1
1
NAND
0
(d)
collapsed stuck-at faults
non-collapsed stuck-at faults

Figure 7

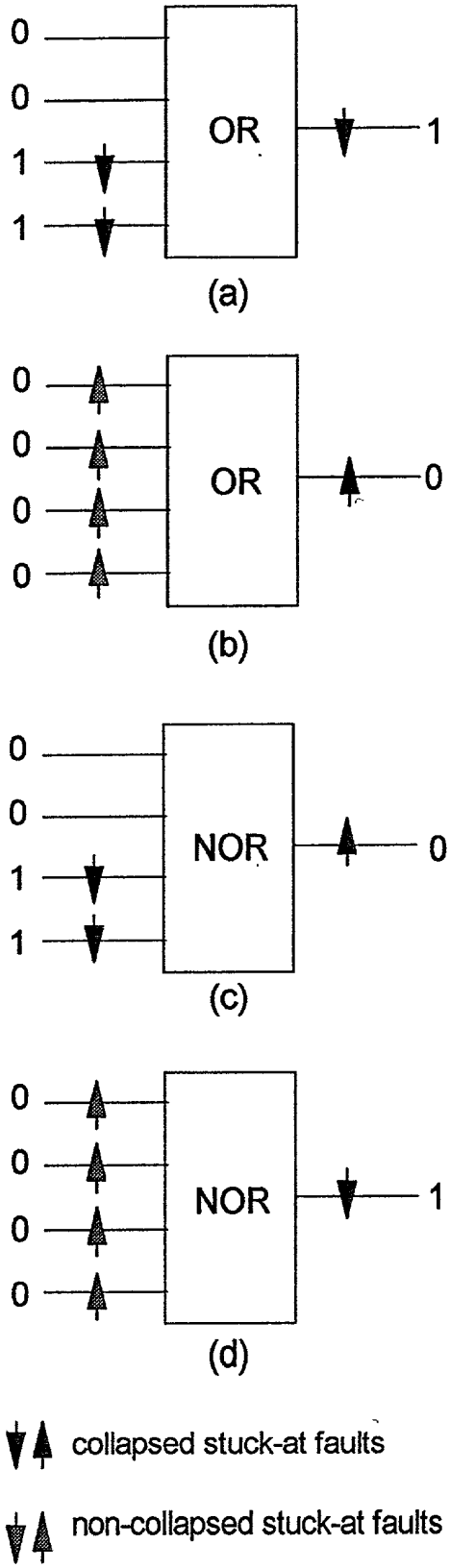
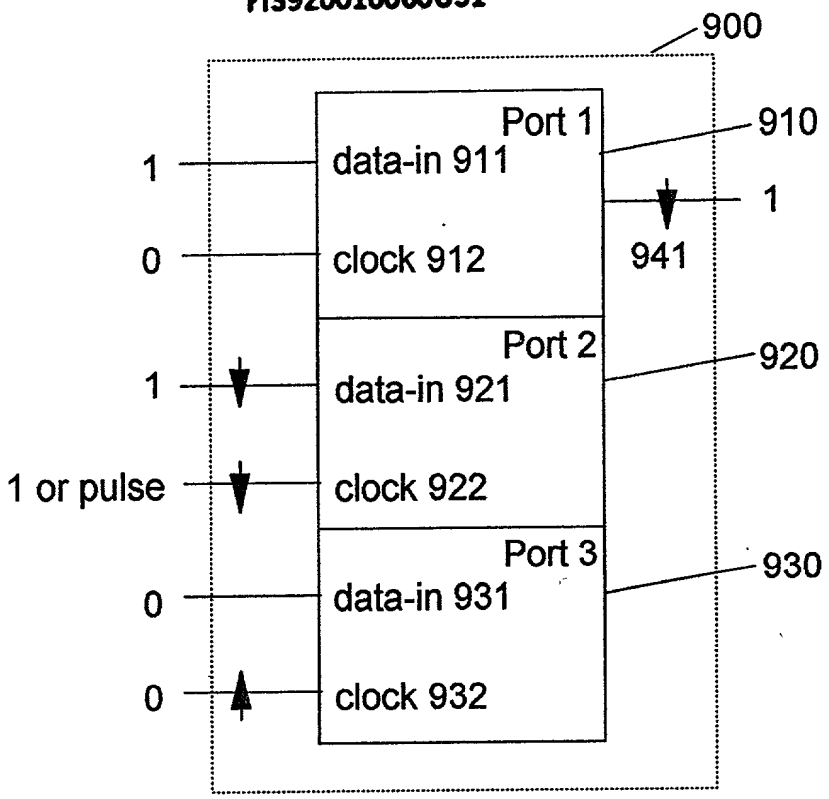
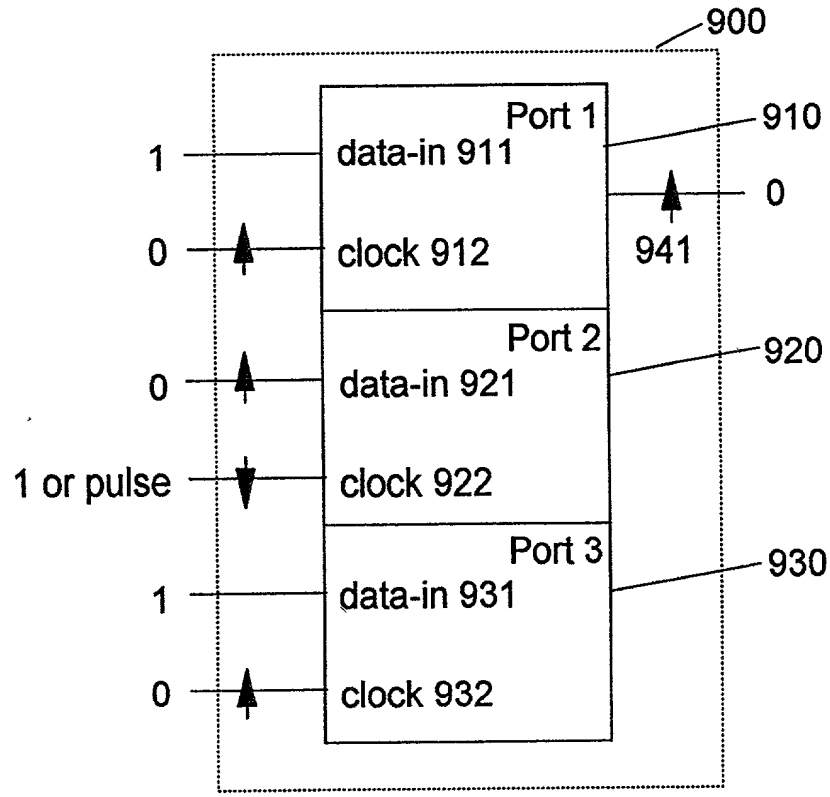

0
0
1
1
OR
1
(a)
0
0
0
0
OR
0
(b)
0
0
1
1
NOR
0
(c)
0
0
0
0
NOR
1
(d)
collapsed stuck-at faults
non-collapsed stuck-at faults

Figure 8.

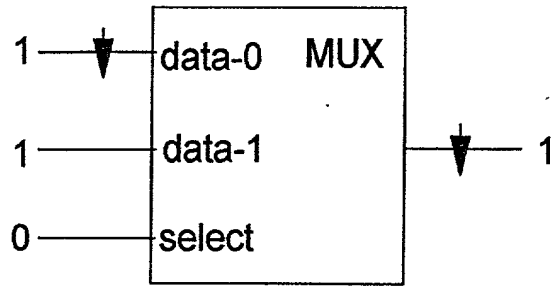

900
Port 1
data-in 911
clock 912
910
1
941
1
0
Port 2
data-in 921
clock 922
920
1
1 or pulse
Port 3
data-in 931
clock 932
930
0
0

(a)

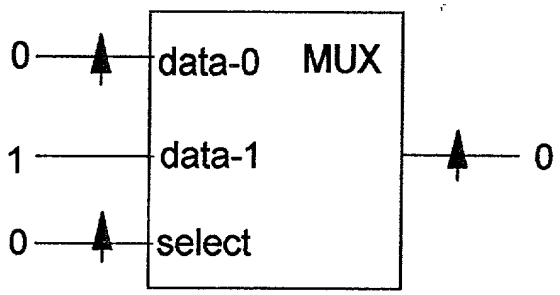

900
Port 1
data-in 911
clock 912
910
0
941
1
0
Port 2
data-in 921
clock 922
920
0
1 or pulse
Port 3
data-in 931
clock 932
930
1
0

(b)

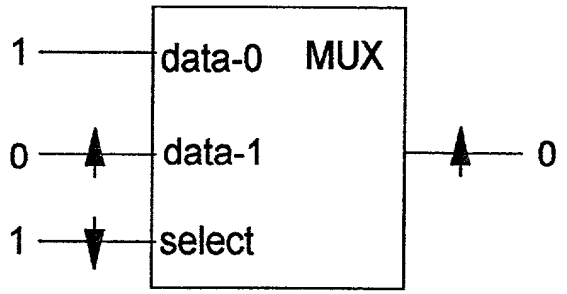
Figure 9.



(a)

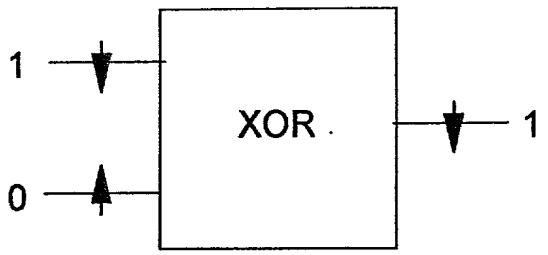


(b)

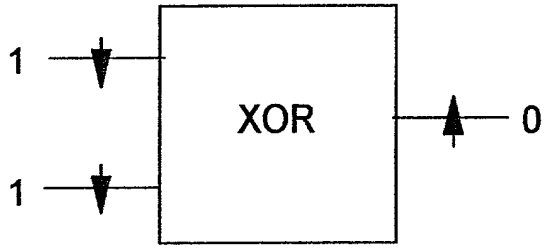


(c)

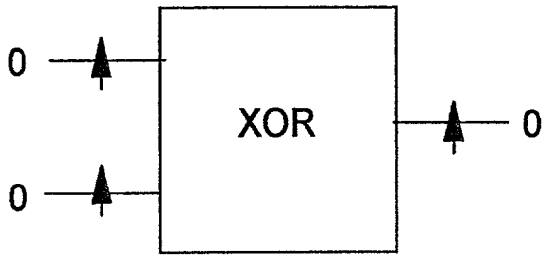
Figure 10.



(a)

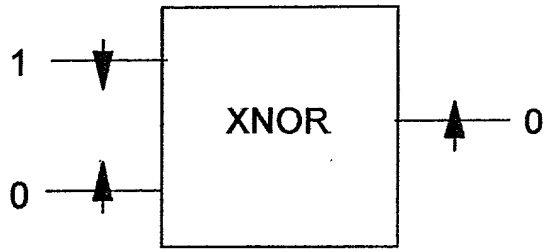


(b)

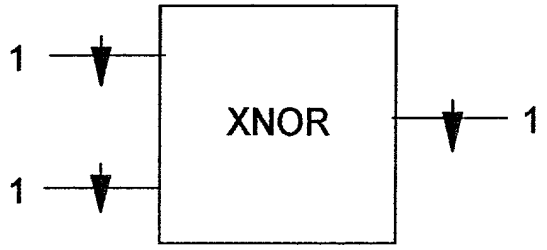


(c)

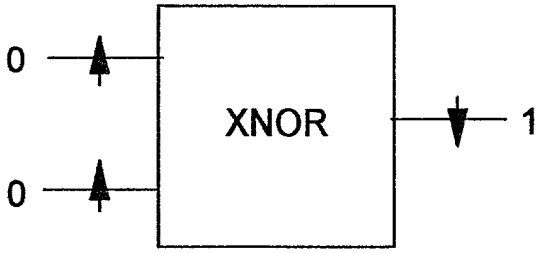
Figure 11.



(a)



(b)



(c)

Figure 12.

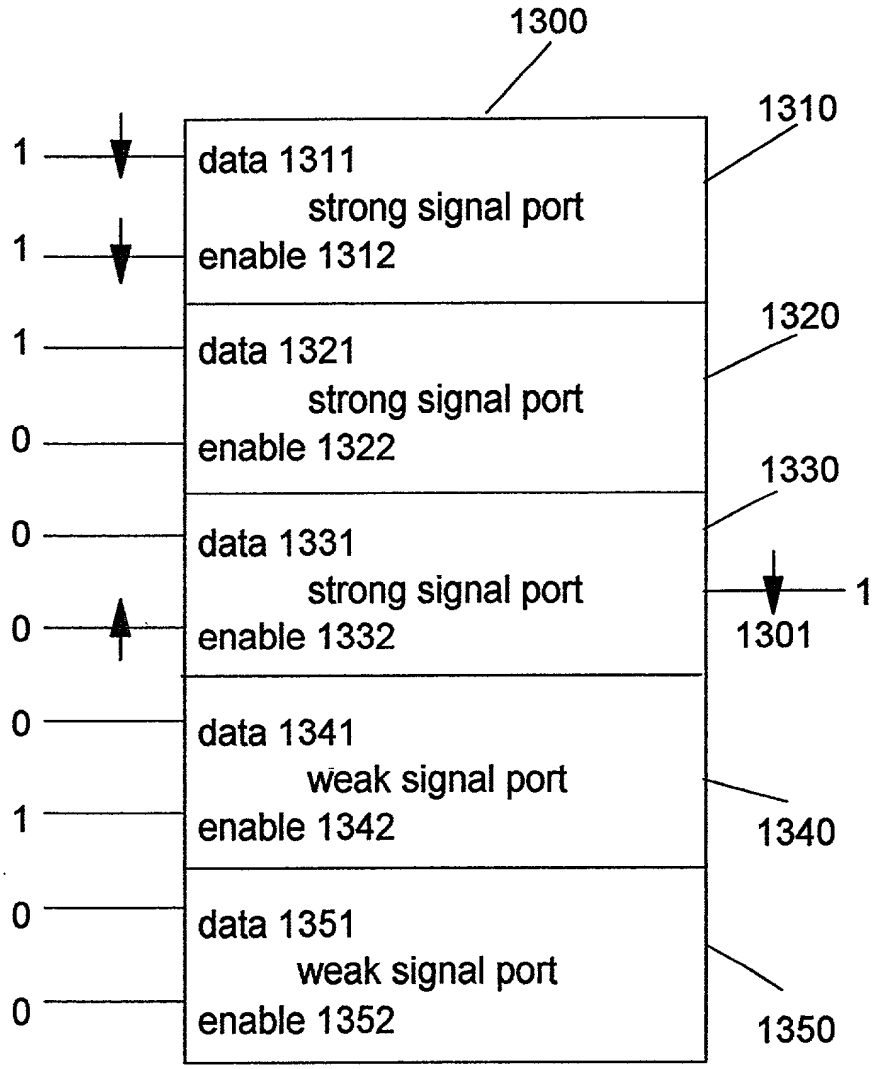

1300
1310
1
data 1311
strong signal port
1
enable 1312
1320
1
data 1321
strong signal port
0
enable 1322
1330
0
data 1331
strong signal port
1
0
enable 1332
1301
0
data 1341
weak signal port
1
enable 1342
1340
0
data 1351
weak signal port
0
enable 1352
1350

Figure 13.

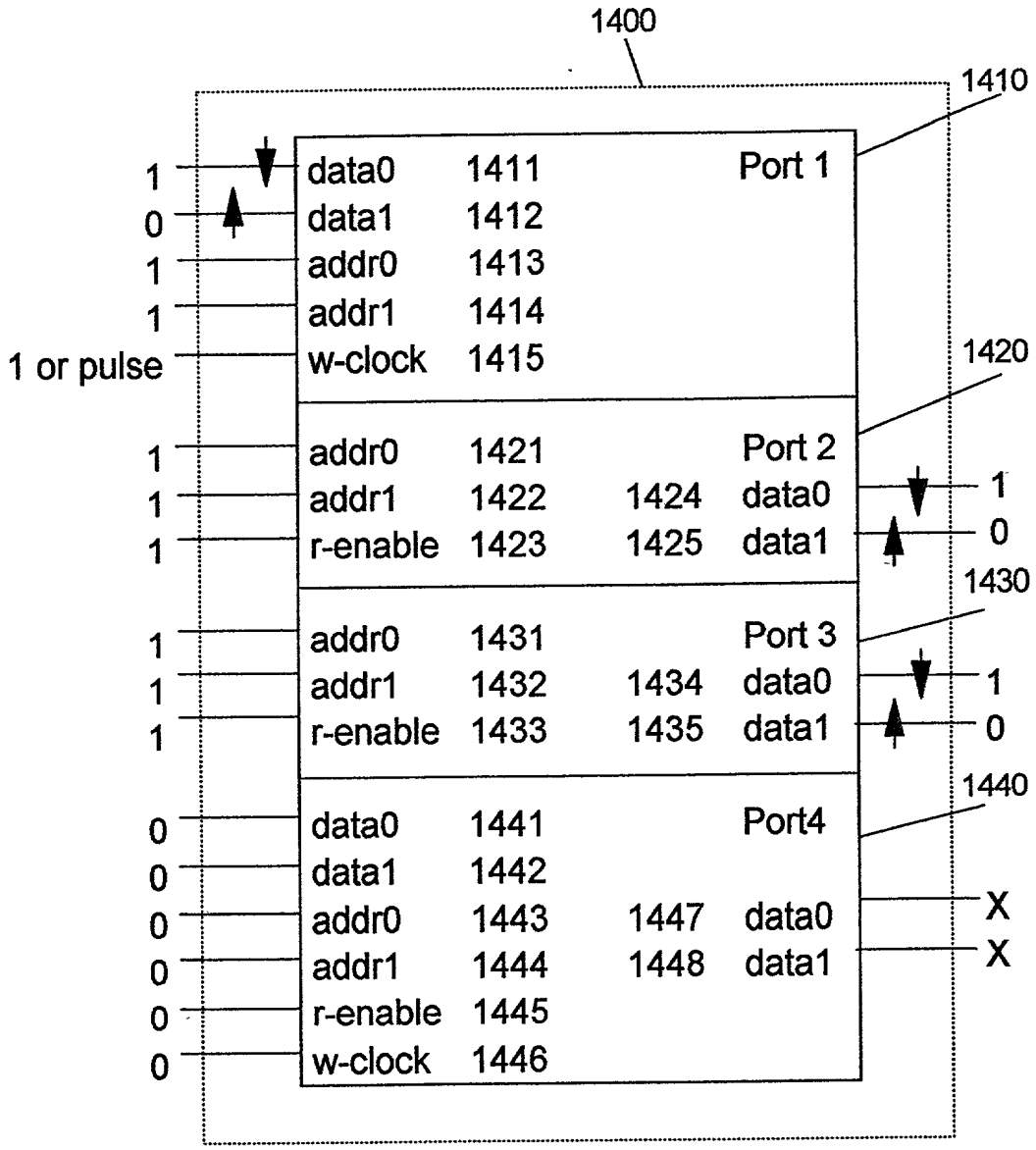

1400
1410
1420
1430
1440
Port 1
data0 1411
data1 1412
addr0 1413
addr1 1414
w-clock 1415
Port 2
addr0 1421
addr1 1422
r-enable 1423
1424 data0
1425 data1
Port 3
addr0 1431
addr1 1432
r-enable 1433
1434 data0
1435 data1
Port4
data0 1441
data1 1442
addr0 1443
addr1 1444
r-enable 1445
w-clock 1446
1447 data0
1448 data1
1 or pulse
X
X

Figure 14.

ROM CONTENT TABLE

addr0	addr1	bit0	bit1
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

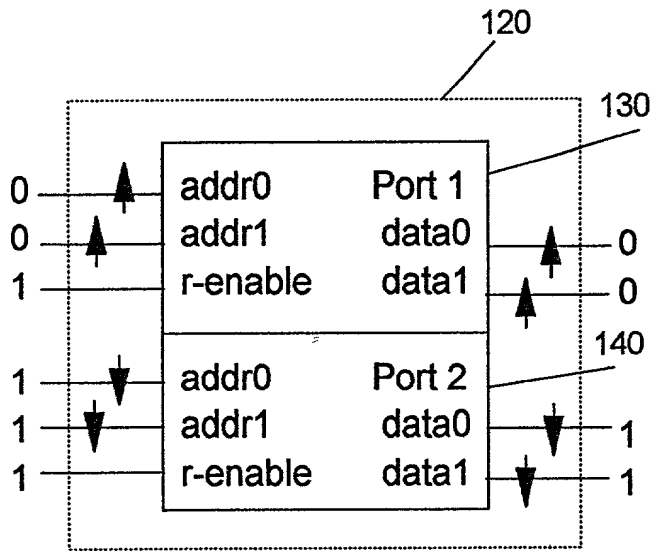


Figure 15.

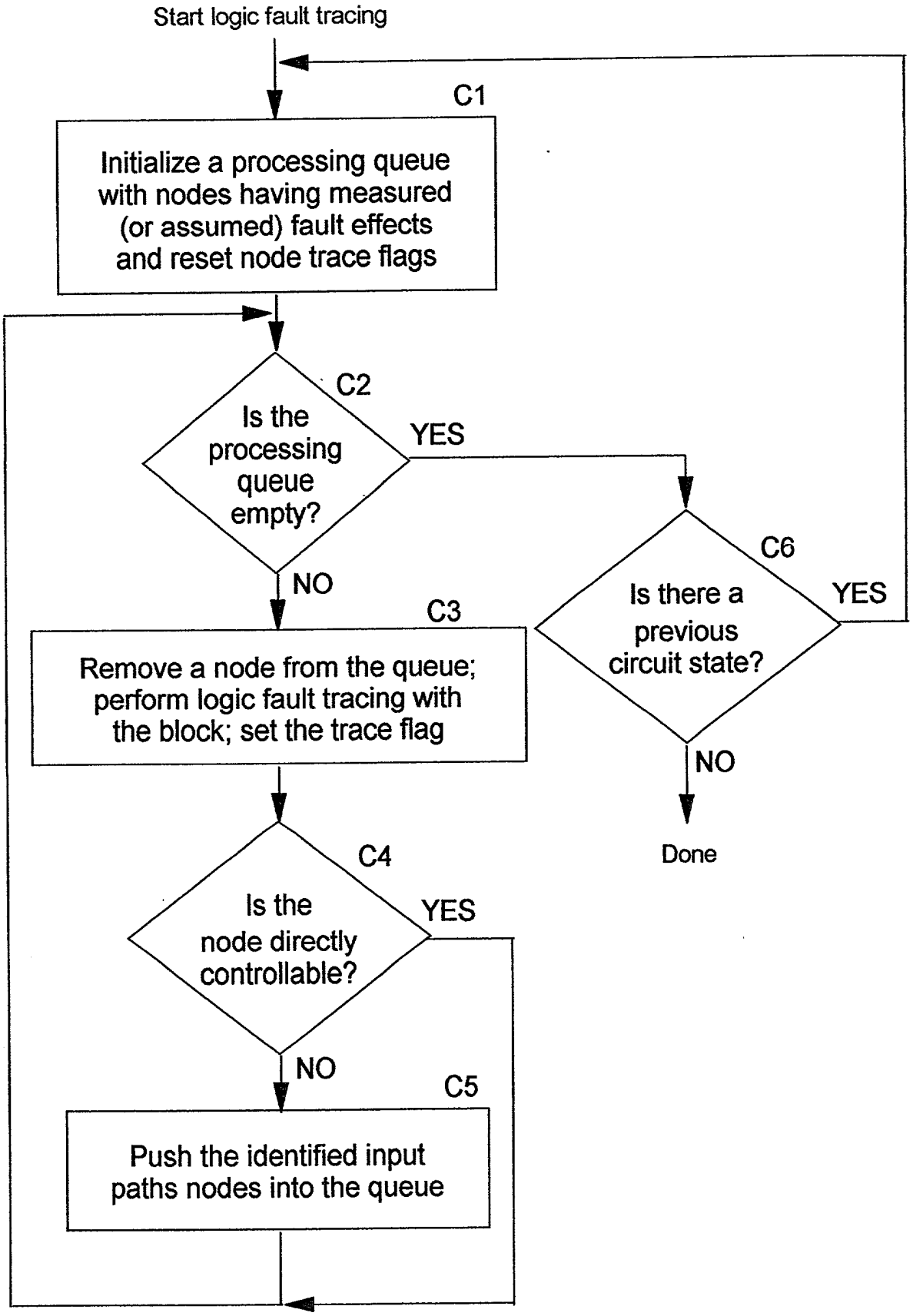

Start logic fault tracing
C1
Initialize a processing queue with nodes having measured (or assumed) fault effects and reset node trace flags
C2
Is the processing queue empty?
YES
NO
C3
Remove a node from the queue; perform logic fault tracing with the block; set the trace flag
C4
Is the node directly controllable?
YES
NO
C5
Push the identified input paths nodes into the queue
C6
Is there a previous circuit state?
YES
NO
Done

Figure 16.

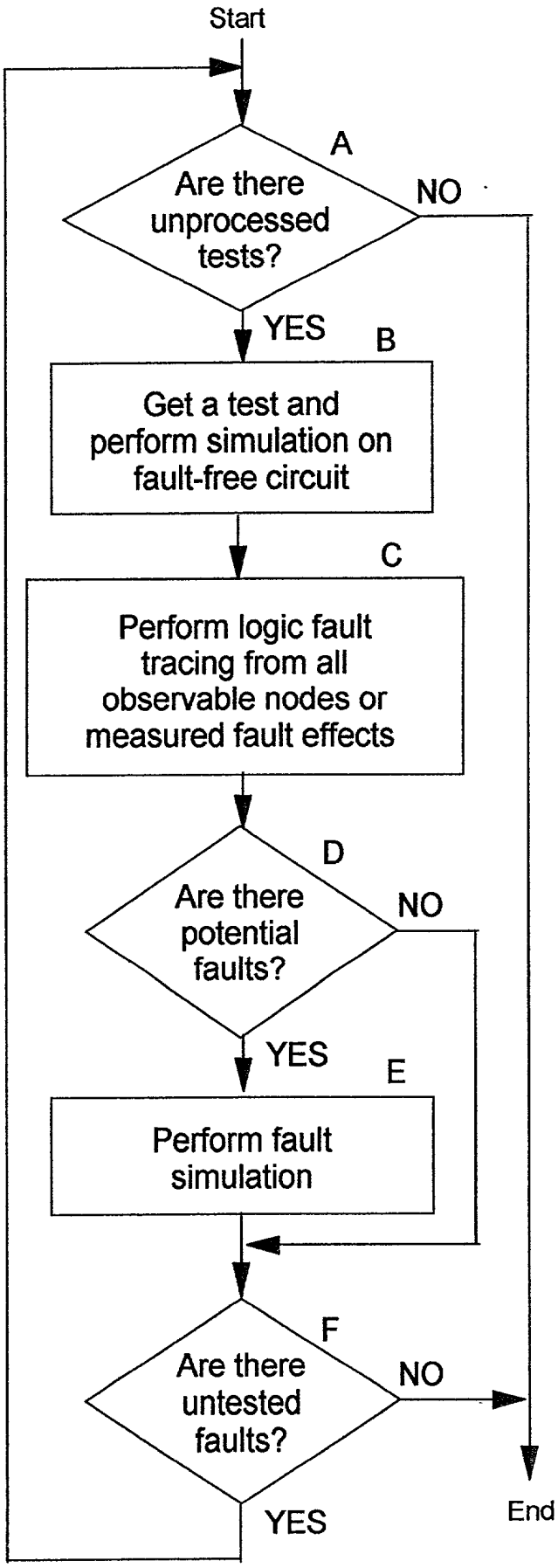

Start
A
Are there unprocessed tests?
NO
YES
B
Get a test and perform simulation on fault-free circuit
C
Perform logic fault tracing from all observable nodes or measured fault effects
D
Are there potential faults?
NO
YES
E
Perform fault simulation
F
Are there untested faults?
NO
YES
End

Figure 17.